

## REMARKS

### A. Introduction

Applicants would like to thank the Examiner for the courtesy extended during the interviews conducted on April 9 and 17, 2008. The interviews clarified several issues and enabled Applicants to better focus the present Amendment to expedite allowance of the present application.

Applicants respectfully request reconsideration and allowance of this application. Claims 1-21 are pending in the application. Applicants respectfully disagree with the Examiner's reasons for rejecting the claims. Nevertheless, Applicants have amended Claims 1, 8 and 15. Applicants' amendments are made for the purpose of expediting further prosecution, and do not in any way indicate Applicants' agreement with the rationale behind the Examiner's rejections. Applicants reserve the right to pursue the original claims, and other claims, in continuing applications.

Applicants have amended Claims 1-22. Applicants' claim amendments are shown on the pages above following the heading AMENDMENTS TO THE CLAIMS. On these pages, the deletions are ~~struckthrough~~ or [[double bracketed]] while the insertions are underlined.

Applicants submit that this application is now in condition for allowance, and Applicants earnestly request such action. Below, Applicants address each of the Examiner's reasons for rejection.

### B. All Claims are Patentable Over the Cited References Rengarajan in view of Nejedlo

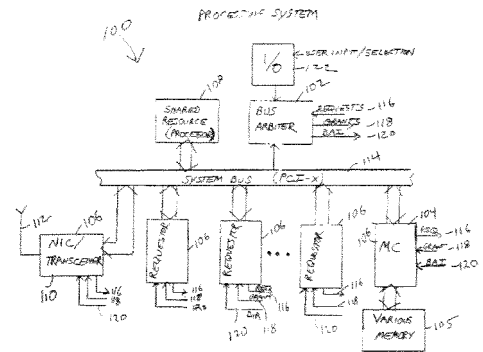
The Examiner rejected Claims 1, 8 and 15 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2005/0060452 to Rengarajan in view of U.S. Patent Application Publication No. 2004/0204912 to Nejedlo et al. ("Nejedlo"). Applicants respectfully submit that these claims are allowable over Rengarajan in view of Nejedlo.

#### Claim 1

Various preferred embodiments of the present application define, *inter alia*, a PCI-Express slot for coupling PCI-Express devices to a host system including a processor. The PCI-Express slot comprises a PCI-Express connector for receiving a card having at least two independent PCI-Express devices. Each independent PCI-Express device uses an independent set of PCI-Express lanes. The PCI-Express slot is located on a motherboard of the host system

and the host system processor communicates with the at least two independent PCI-Express devices via the two independent sets of PCI-Express lanes without using a bridge.

By contrast, Rengarajan discloses a system and method for predicting when to generate a bus request ahead of time based on bus activity, bus usage efficiency and bus bandwidth usage. With reference to Figure 1 of Rengarajan, reproduced at right, Rengarajan does not teach or suggest at least a PCI-Express connector for receiving a card having at least two independent PCI-



Express devices, wherein each independent PCI-Express device uses an independent set of PCI-Express lanes, and further wherein a host system processor communicates with the at least two independent PCI-Express devices via the two independent sets of PCI-Express lanes without using a bridge. With further reference to Figure 1 of Rengarajan, none of the requestors 106 connected to the system bus 114 meets all of these limitations. Nejedlo, which discloses only a serial bus testing methodology, also does not teach or suggest all of the above limitations.

Since neither Rengarajan nor Nejedlo, nor their combination, teaches or suggests a PCI-Express connector as recited in Claim 1, Applicants respectfully submit that independent Claim 1 is allowable over Rengarajan in view of Nejedlo. Accordingly, Applicants respectfully request that the Examiner withdraw this rejection.

#### Claim 8

Various preferred embodiments of the present application define, *inter alia*, a system for coupling plural PCI-Express devices to a host system including a processor. The system comprises a motherboard with a PCI-Express slot having a PCI-Express connector configured to receive a card having at least two independent PCI-Express devices. Each independent PCI-Express device uses an independent set of PCI-Express lanes. The host system processor communicates with the at least two independent PCI-Express devices via the two independent sets of PCI-Express lanes without using a bridge.

By contrast, Rengarajan discloses a system and method for predicting when to generate a bus request ahead of time based on bus activity, bus usage efficiency and bus bandwidth usage, as described above. As further described above, Rengarajan does not teach or suggest at least a PCI-Express connector configured to receive a card having at least two independent PCI-Express

devices, wherein each independent PCI-Express device uses an independent set of PCI-Express lanes, and further wherein a host system processor communicates with the at least two independent PCI-Express devices via the two independent sets of PCI-Express lanes without using a bridge. As further described above, Nejedlo similarly fails to teach or suggest these limitations.

Since neither Rengarajan nor Nejedlo, nor their combination, teaches or suggests a PCI-Express connector as recited in Claim 8, Applicants respectfully submit that independent Claim 8 is allowable over Rengarajan in view of Nejedlo. Accordingly, Applicants respectfully request that the Examiner withdraw this rejection.

Claim 15

Various preferred embodiments of the present application define, *inter alia*, a PCI-Express connector in a PCI-Express slot on a mother board of a host system. The host system includes a processor. The connector is configured to receive a card having at least two independent PCI-Express devices to couple the independent PCI-Express devices to the host system. Each independent PCI-Express device uses an independent set of PCI-Express lanes. The host system processor communicates with the at least two independent PCI-Express devices via the two independent sets of PCI-Express lanes without using a bridge.

By contrast, Rengarajan discloses a system and method for predicting when to generate a bus request ahead of time based on bus activity, bus usage efficiency and bus bandwidth usage, as described above. As further described above, Rengarajan does not teach or suggest at least a PCI-Express connector configured to receive a card having at least two independent PCI-Express devices, wherein each independent PCI-Express device uses an independent set of PCI-Express lanes, and further wherein a host system processor communicates with the at least two independent PCI-Express devices via the two independent sets of PCI-Express lanes without using a bridge. As further described above, Nejedlo similarly fails to teach or suggest these limitations.

Since neither Rengarajan nor Nejedlo, nor their combination, teaches or suggests a PCI-Express connector as recited in Claim 15, Applicants respectfully submit that independent Claim 15 is allowable over Rengarajan in view of Nejedlo. Accordingly, Applicants respectfully request that the Examiner withdraw this rejection.

Rengarajan in view of Gonzalez

The Examiner rejected Claims 2-7, 9-14 and 16-21 under 35 U.S.C. § 103(a) as being unpatentable over Rengarajan in view of U.S. Patent Application Publication No. 2005/0088445 to Gonzalez et al. ("Gonzalez"). Claims 2-7, 9-14 and 16-21 each depend from Claims 1, 8 and 15, respectively, and therefore include all of the limitations of Claims 1, 8 and 15, respectively. Claims 1, 8 and 15 are allowable over Rengarajan for the reasons provided above. Claims 1, 8 and 15 are also allowable over Rengarajan in view of Gonzalez, because Gonzalez neither teaches nor suggests the limitations of Claims 1, 8 and 15 that are lacking in Rengarajan. Accordingly, Claims 2-7, 9-14 and 16-21 are all allowable for at least the same reasons provided above with respect to Claims 1, 8 and 15, and Applicants respectfully request that the Examiner withdraw these rejections.

**CONCLUSION**

For the reasons presented above, Applicants respectfully submit that this application, as amended, is in condition for allowance. If there is any further hindrance to allowance of the pending claims, Applicants invite the Examiner to contact the undersigned.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1159.

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Respectfully submitted,



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